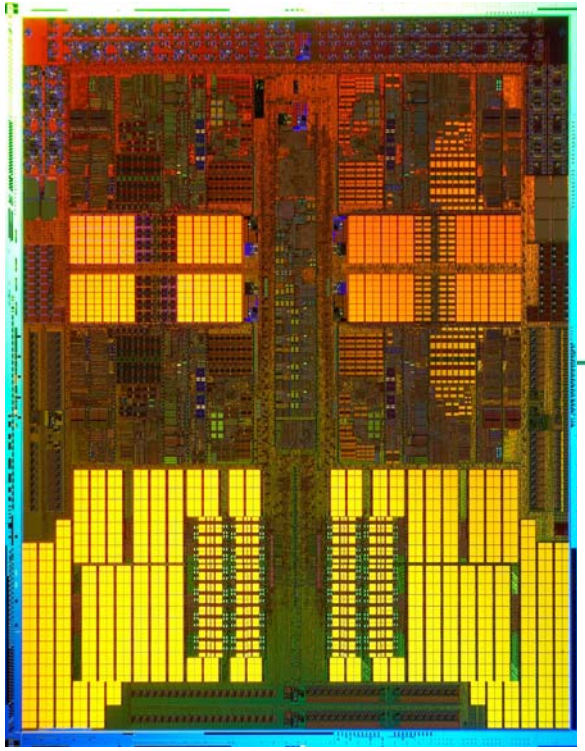
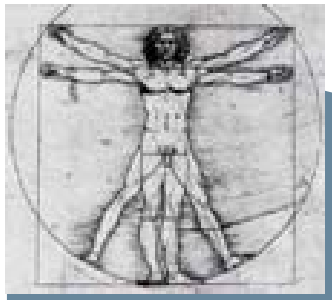


45nm Quad-Core

AMD
Smarter Choice

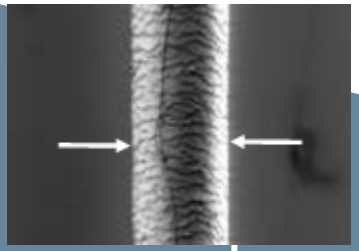
Manufacturing and Process Technology Update

Macroscale to Nanoscale – Feature Sizes

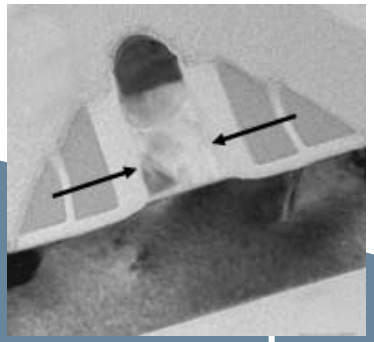


Man: ~2 m
= 2,000,000,000 nm

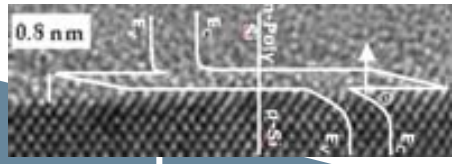
Human Hair:
60,000 nm



Transistor Gate: 40 nm

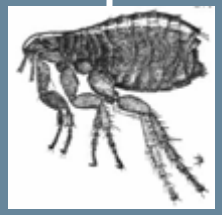


High-Performance
Gate Oxide: 0.8 nm

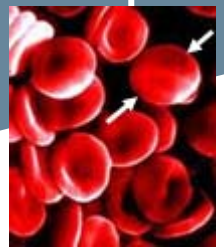


cm mm µm nm

10^{0} 10^{-1} 10^{-2} 10^{-3} 10^{-4} 10^{-5} 10^{-6} 10^{-7} 10^{-8} 10^{-9} 10^{-10} 10^{-11}

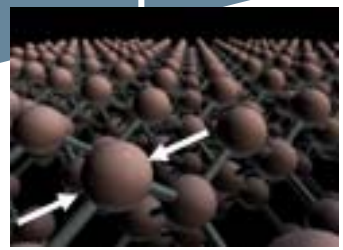


Flea: ~1 mm
= 1,000,000 nm



Blood Cell:
7,500 nm

DNA: 3.4 nm



Silicon Atom:
0.22 nm

AMD's History of Semiconductor Manufacturing Process Innovations

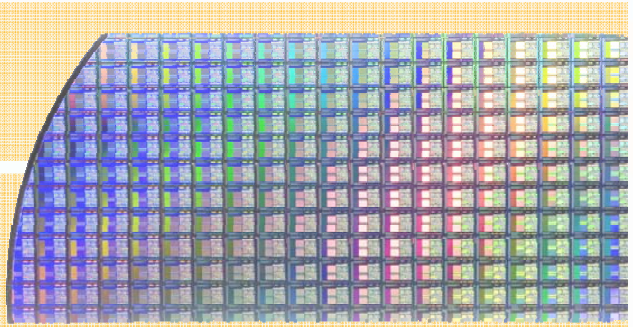
- First company to volume production with copper metal interconnect as replacement for aluminum
- First microprocessor vendor to insert immersion lithography into its fab tool set
- First to apply strained silicon across a range of strain intensities on same transistor
- First to volume production with low-K interconnect material
- First "full field" demonstration of Extreme Ultra Violet (EUV) lithography resulting in working test chip

AMD & 45nm
Fueling continuous technology innovation

AMD Smarter Choice

Jointly Developed

- Jointly developed by IBM and AMD



Production Efficiency

- Ramped Immersion lithography
  - Addresses unique needs of finer geometry
  - Eliminates need for double exposures to reduce cost and complexity

Performance and Power Efficiency

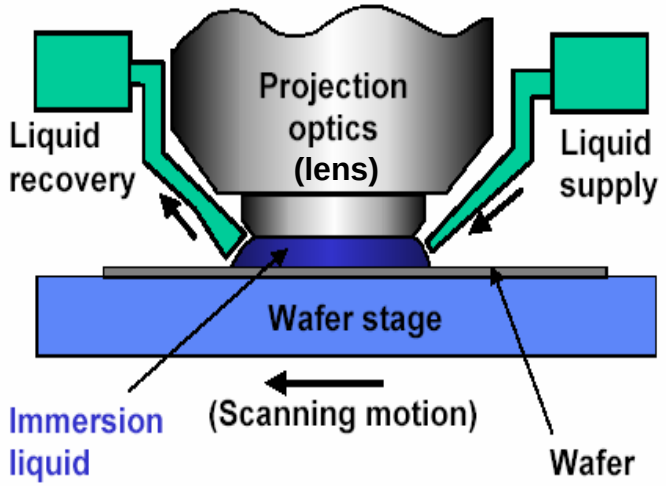
- 20 percent performance improvement from strained silicon and ultra-low-K dielectrics
- High-k/metal gate / future 45nm option
- Continuous Transistor Improvements (CTI) applied throughout life-cycle of the process

Immersion Lithography
Improving the manufacturing process

AMD Smarter Choice

Lithography For 45nm

- Immersion effectively decreases wavelength by putting water between the projection lens and the silicon wafer
  - If a fluid of refractive index n fills the space between the lens and the wafer, then the effective wavelength = the vacuum wavelength of the light ÷ by n
  - For air, n is approximately equal to 1.0
  - For water, n is approximately equal to 1.4 because water is denser than air
- Shorter effective wavelengths enable smaller features to be patterned



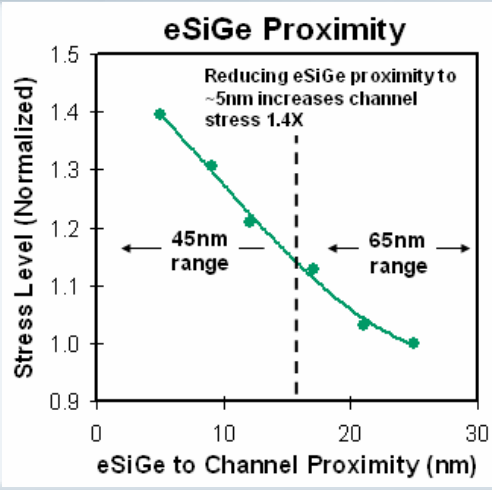
40 percent gain in resolution over conventional lithography

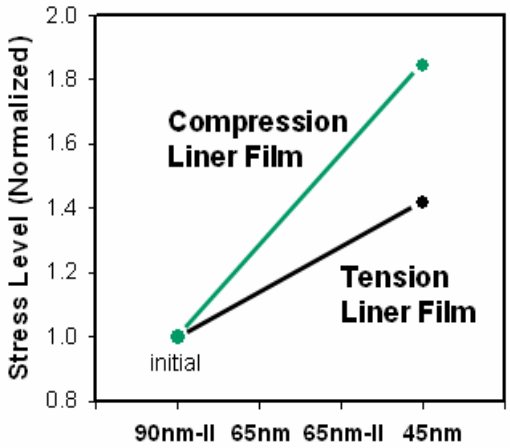
Advancements in Strain Engineering
45nm

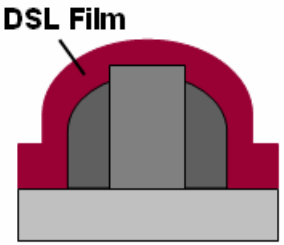
AMD Smarter Choice

Scaling to 45nm pitch impacts stress effectiveness

Dual Stress Liner and embedded SiGe techniques have been enhanced and extended in response

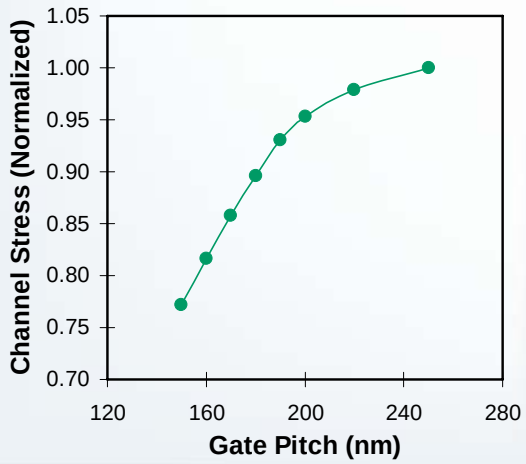






Since DSL introduction stress has been enhanced:

- 1.9X for PFET film
- 1.4X for NFET film



Ultra-Low-K Interconnect Dielectric

Improving circuit speed and reducing power

AMD Smarter Choice

Decreases capacitance of insulator surrounding copper wires by introducing pores into the insulator material

Capacitance depends on the dielectric constant (k) of the insulator

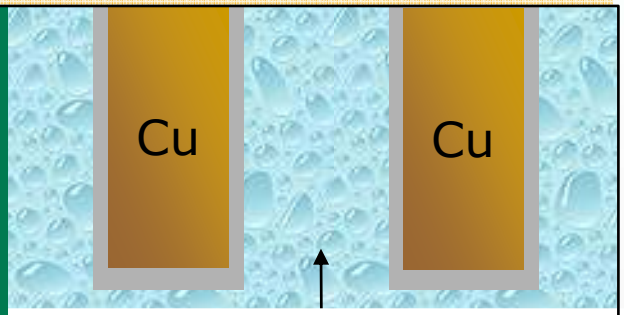
- Current low-k dielectric materials have k = 3.0

Introducing pores (air) throughout the insulator further lowers k

- Reduces the k to 2.4
- Unique integration for improved yield and reliability

A superior ultra-low-k (ULK; k = 2.4) film, manufacturing process and tool set were developed for 45nm

- Elements were integrated successfully to build wiring suitable for advanced, high-performance microprocessors
- Extensive testing was used to establish manufacturing robustness and chip reliability



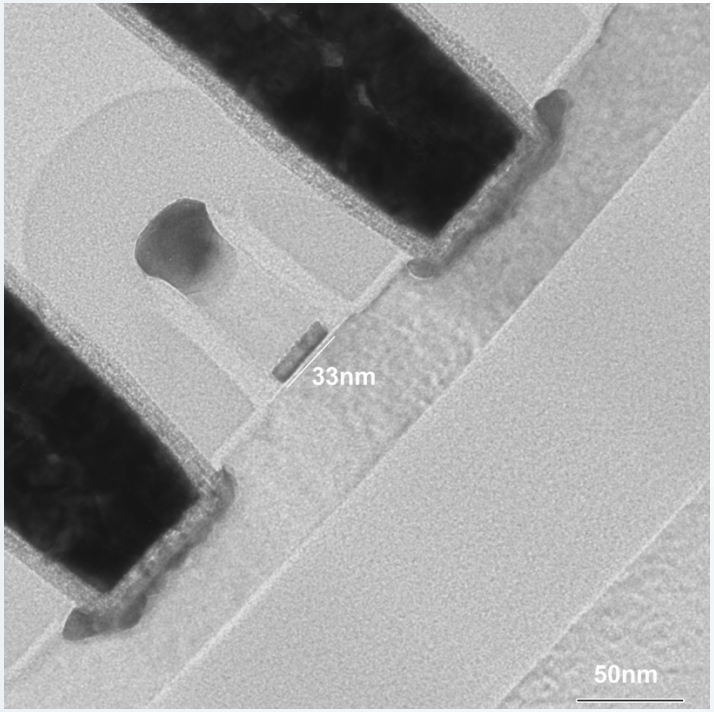
Pores in dielectric
(Artistic Representation)

AMD & High-k / Metal Gate Transistors

AMD
Smarter Choice

Unique High-k/Metal Gate Approach, Consistent Results

- "Gate First" approach minimizes complexity and cost — consistent with current technology
- Reduces capacitance for lower power and improved performance over other approaches
- Improves device performance through mobility enhancement
- Supports scaling, performance improvements at 32nm node, future option for 45nm



AMD Quantifies Design for Manufacturability (DFM)

AMD Smarter Choice

Integrated & automated set of methodologies measure DFM Results Across Entire Chip

Automated

- Rapid specification of design margins
- Translation across database structures (design to fab)
- AMD's Automated Precision Manufacturing (APM) adjusts to new specifications

Integrated

- Defined by fab, implemented by design tools, results measured
- Allows exchange of design data
- Enables exchange of silicon data

DFM Results Applied to Process / Design in Real-Time

AMD Dresden
- Continuing to Set the Standard

AMD
Smarter Choice

Fab 36

- 300mm microprocessor fab
- Fully Equipped / Q4, 2007
- Aggressively transitioned to 65nm
- Ramped 65nm at mature yields with extremely low defect densities
- 45nm Line Ramping 1H 2008, 2H Production

Fab 38

- Leverages award winning Fab30 clean room
- Pioneer in Lean manufacturing techniques
- Qualified 300mm tools supporting Fab36 production in 2008
- Transition to stand-alone 300mm factory in 2009

New Bump and Test Facility Operational

In Summary

AMD continues to execute on process technology transitions

AMD's co-development with IBM (and partners) is a smart approach to advanced R&D

AMD's process technology roadmap is driven by end-user benefits